ABSTRACT OF THE DISCLOSURE

Systems and methods to implement an improved floating point adder are presented. The adder integrates adding and rounding. According to an exemplary method, of adding two floating point numbers together, a first mantissa, a second mantissa, and an input bit are added together to produce a third mantissa. The third mantissa is normalized to produce a final mantissa. The third mantissa and the final mantissa are correctly rounded as a result of the act of adding, so that the final mantissa does not require processing by a follow on rounding stage.